ABSTRACT OF THE DISCLOSURE

A method for fabricating a vertical nitride read-only memory (NROM) cell. A substrate having at least one trench is provided. A spacer is formed over the sidewall of the trench. Subsequently, ion implantation is performed on the substrate using the spacer as a mask to form doping areas as bit lines in the substrate near its surface and the bottom of the trench. Bit line oxides are formed over each of the doping areas. After the spacer is removed, a conformable insulating layer as gate dielectric is deposited on the sidewall of the trench and the surface of the bit line oxide. Finally, a conductive layer as a word line is deposited over the insulating layer and fills in the trench.